DASP-52282

12-bit 330KHz Multifunction w/ Free-Running Card

User's Manual

Disclaimers

The information in this manual has been carefully checked and is believed to be accurate. Axiomtek Co., Ltd. assumes no responsibility for any infringements of patents or other rights of third parties which may result from its use.

Axiomtek assumes no responsibility for any inaccuracies that may be contained in this document. Axiomtek makes no commitment to update or to keep current the information contained in this manual.

Axiomtek reserves the right to make improvements to this document and/or product at any time and without notice.

No part of this document may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of Axiomtek Co., Ltd.

September 2004, Version A1.0
Printed in Taiwan

ESD Precautions

Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.

Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.

Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

Trademarks Acknowledgments

Table of Contents

Chapter 1 Introduction 1
1.1 Features 2
1.2 Specifications 3
1.3 Accessories 5

Chapter 2 Hardware Installation 7
2.1 Board Layout 7
2.2 Signal Connections 8
2.2.1 Signal Connection Descriptions 8
2.2.2 Digital Input Connector CON1 9
2.2.3 Digital Output Connector CON2 11
2.2.4 A/D, D/A and Timer/Counter Connector CON4 13
2.3 Jumper Setting 16
2.3.1 ADC Clock Source (JP4) 16
2.3.2 DAC1, DAC2 Output Range Selection (JP8 and JP9) 16
2.3.3 A/D Single-Ended / Differential Selection (JP1) . 16
2.4 A/D, D/A and DI/DO Circuits and Wiring 17
2.5 Quick setup and test 19

Chapter 3 Theorem of Operation 25
3.1 Overview of DASP-52282 System Architecture and Operation 25
3.2 Acquisition Modes of Analog Input 26
3.2.1 Polling Mode 26
3.2.2 Pacer Mode 26
3.2.3 External Trigger Mode 27
3.3 Double Buffering Mechanism For Fast Data Acquisition 30
3.3.1 On Board FIFO and FIFO Half Full Interrupt 30
3.3.2 Circular Buffer for Massive Data Buffering 32
3.4 Automatic Scan 32
3.5 Analog Input Range, ADC Code and AD Value .. 33

Chapter 4 Register Structure and Format 37
4.1 Overview 37
4.2 I/O Register Map 38
4.2.1 Digital Input Buffer Register 38
4.2.2 Digital Output Latch Register 38

4.2.3 General Status Buffer Register..... 38
4.2.4 Command Output Latch Register 40
4.2.5 A/D Data Register 43
4.2.6 DAC Channel 1 Output Latch Register..... 43
4.2.7 A/D FIFO Data Register..... 43
4.2.8 DAC Channel 2 Output Latch Register..... 44
4.2.9 8254 Timer/Counter Register..... 44
4.2.10 8254 Timer/Counter Control Words Register..... 44
4.2.11 Clear FIFO Content Register..... 45
4.2.12 Clear Flag Register 45
4.2.13 Enable DAC1 and DAC2 Output Register 45
4.2.14 A/D ADC Software Polling Control Register..... 46
4.2.15 Enable ADC Register 46
4.2.16 Disable ADC Register..... 46

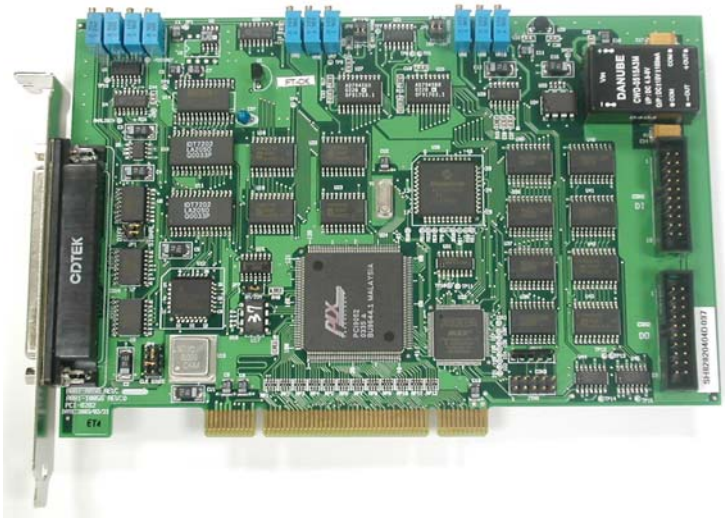
Chapter 5 Calibration 47
5.1 Calibration VR Description.....47
5.2 D/A Calibration 48
5.3 A/D Calibration Steps 48

Appendix A Analog Input Gain Mode Configuration 49

Appendix B Dimension of DASP-52282 and Accessories 51

This page does not contain any information.

Chapter 1
Introduction



The DASP-52282 is a high performance, PCI bus multi- function card. It supports a 330KHz sampling rate, 16 single-ended or 8 differential AI, 16DI, and 16 DO. The DASP-52282 also features an all new free-running mechanism to reduce the S/W development efforts, and provides high/low gain options for user's applications.

Advanced S/W Mechanism: Free-running

Free-running is a brand new data-retrieving mechanism to mainly save software SW RD 30% -- 50% of the time and effort in developing application programs. It helps software RD by using several rows of simple programs to read data, instead of countless numbers in the past.

Board identification- Serial Number on EEPROM

The DASP stores the serial number of each DASP in the EEPROM before shipping. The PCI scan utility can scan all the DASP and show users the serial number of each DASP, helping the user to easily identify and access each card.

Easily Developing Application Programs-Various Sample Programs

The DASP-52282 series provides many user-friendly sample programs to help users developing various application programs in different units, such as VB, VC, BCB, and Delphi. And it also supports the most popular Labview 6.0/7.0 drivers. The API of the DASP-52282 has passed strict assembling tests that helps users not necessarily writer such complicated and wordy programs while using it.

Easy to Troubleshoot Hardware Resource- PCI Scan Utility

The PCI scan utility can scan all the DASP products within the system, and can show users all system resources, such as serial numbers, IRQ, and I/O addresses. This lets users clearly see through and immediately know whether all DASPs are working normally, decreasing the time of searching confirmation.

- **DASP-52282:**
  12-bit, 330 KHz multifunction board
- **DASP-52282L:**
  12-bit, 330 KHz multifunction board w/o DAC
- **DASP-52282H:**
  12-bit, 330 KHz high-gain multifunction board
- **DASP-52282HL:**
  12-bit, 330 KHz high-gain multifunction board w/o DAC

1.1 Features

- **2 channel 12-bit D/A voltage output**
- **16 D/I and 16 D/O (TTL compatible)**
- **Maximum sampling rate up to 330KHz**
- **Supports free-running mechanism with 1K FIFO**
- **A/D trigger mode: software trigger, pacer trigger, external trigger**
- **Supports software programmable gain**
- **Supports Windows® 98/NT/2000/XP, Labview 6.0/7.0 driver**
- **Supports VB, VC, BCB, Delphi sample program**

1.2 Specifications

Analog to Digital Converter (A/D)

- **Channels: 16 Single-ended or 8 differentials**
- **Resolution: 12-bit**
- **FIFO size: 1K samples**
- **Sampling Rate: 330KS/s max.**
- **Conversion Time: 3μ s**
- **ADC input range: ±10V**
- **Input protect: 30 Vp-p**
- **On chip sample and hold.**
- **Programmable Gain**
  - Low Gain (DASP-52282/ DASP-52282L only)

Gain	0.5	1	2	4	8
Unipolar	N/A	0~10V	0~5 v	0~2.5v	0~1.25v
Bipolar	±10V	±5v	±2.5v	±1.25v	±0.625v

  - High Gain (DASP-52282H/ DASP-52282HL)

Gain	0.5	1	10	100	1000
Unipolar	N/A	0~10V	0~1V	0~0.1V	0~0.01V
Bipolar	±10V	±5v	±0.5V	±0.05V	±0.005V

- **Small signal bandwidth for PGA:**
  - Low Gain (DASP-52282/ DASP-52282L only)

Gain	0.5	1	2	4	8
Bandwidth	5MHz	5 MHz	4 MHz	1.3 MHz	600 KHz

  - High Gain (DASP-52282H/ DASP-52282HL only)

Gain	0.5	1	10	100	1000
Bandwidth	1MHz	1 MHz	80 KHz	10 KHz	1 KHz

- **Drift: 0.1 LSB @ gain 0.5**
- **Max. input voltage: ±20V**
- **Input impedance: 10000 MΩ | 6 pF**
- **On chip sample and hold**

- **AD Trigger Method:**
  Software, Pacer, External
  (Pre-trigger, Post trigger, Middle trigger)
- **Analog Input Data Transfer Method:**
  Polling, Interrupt, FIFO
- **Operation mode:**
  Polling mode, Pacer mode, Interrupt mode,
  External pre-trigger mode,
  External post trigger mode,
  External middle trigger mode
- **DC Accuracy:**
  INL: +/- 1 LSB @ gain 0.5
  DNL: +/- 1LSB @ gain 0.5
- **AC Accuracy: SNR: 71dB @ gain 0.5**
- **Automatic Scan Mechanism**

Digital to Analog Converter (D/A) (only DASP-52282 / DASP-52282H)

- **Channels: 2 independent**
- **Resolution: 12-bit, analog device AD7945BR**
- **Output range:**
  Bipolar: -9.9998V ~ 10.0003V @ -10~+10V
  Unipolor: 0.0003V ~ 10.0002V @ 0 ~ 10V
- **Accuracy: +/- 0.5 LSB**
- **Offset: 1%**
- **Slew Rate: 13V/μs**
- **Drift: +/- 0.5 LSB**
- **Output Driver: ±5mA**
- **Max. Transfer Rate: 20μ S/s**
- **Output Impendence: 15 Ω**
- **Settling Time: 0.6 ns to 0.01% for Full Scale Step**
- **Linearity: ±1/2 bit**

Digital I/O

	Digital Input	Digital Output
Channel	16	16
Type	TTL level	TTL level
Voltage low	VIL = 0.8V max. IIL =-0.4mA max.	VOL = 0.5V max @IOL =8mA max.
Voltage high	VIH = 2.0V min. IIH = 20 A max.	VOH = 2.7V min @IOH =-400A max.

1.3 Accessories

To make the DASP-52282 functionality complete, we carry a versatility of accessories for different user requirements in the following items:

Wiring Cable

- **CB-89037-2:**
  37-pin female D-sub type cable with 2m length
- **CB-89037-5:**
  37-pin female D-sub type cable with 5m length
  The shielded D-sub cable with 2m and 5m are designed for the DASP-52282 analog I/O connector, respectively.
- **CB-89320-2:**
  20-pin female flat type cable with 2m length
- **CB-89320-5:**
  20-pin female flat type cable with 5m length
  The flat cable with 2m and 5m are designed for the DASP-52282 digital I/O connector, respectively.

Terminal Block

- **TB-88037:**
  D-sub 37P female terminal block with DIN-rail mounting
  The terminal block is directly connected to analog I/O connector of the DASP-52282.

- **TB-88320:**
  Flat type 20P female terminal block with DIN-rail mounting

  The terminal block is directly connected to D/I or D/O connector of the DASP-52282.

Daughter Board

- **DB-87822:**
  16 isolated D/I daughter board

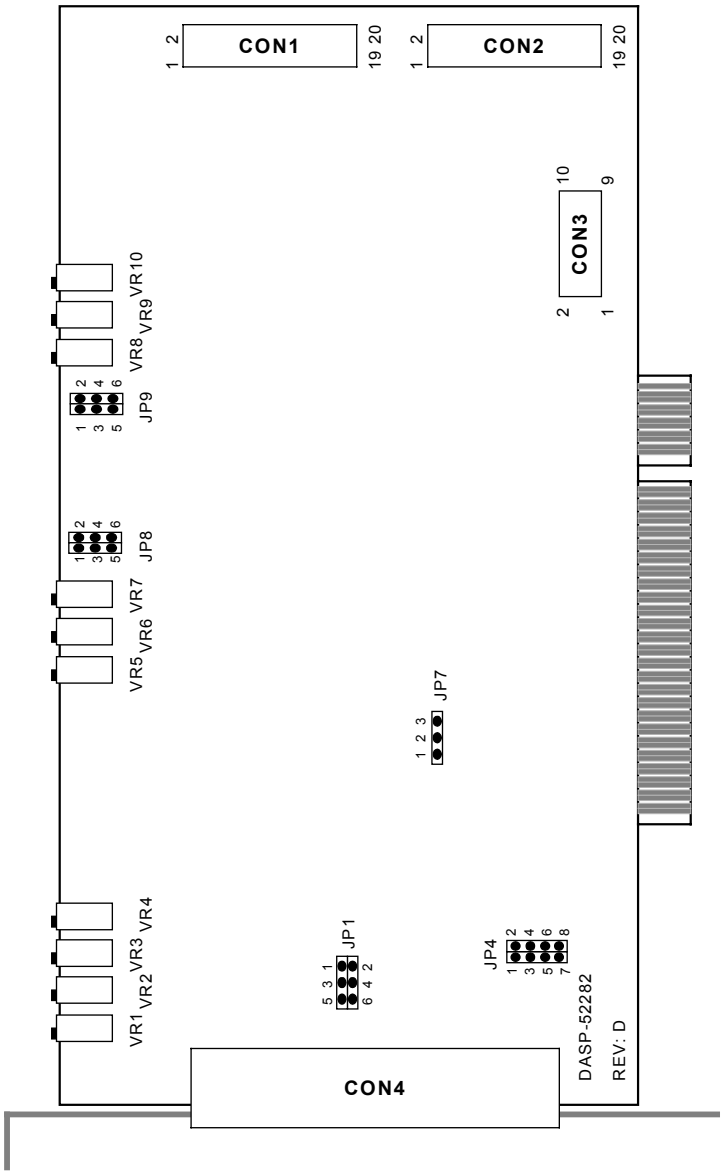
  The board contains 16 channels isolated digital input which is designed for TTL level digital input signal to the DASP-52282.

- **DB-87825:**
  16 relay D/O daughter board

  The board contains 16 channels relay output which is driven by TTL level digital output signal of the DASP-52282.

Chapter 2
Hardware Installation

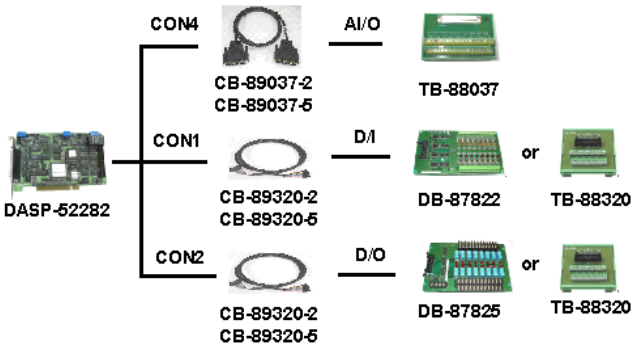
2.1 Board Layout



Board Layout for DASP-52282

2.2 Signal Connections

2.2.1 Signal Connection Descriptions

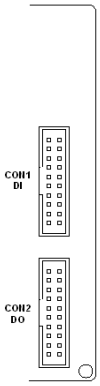


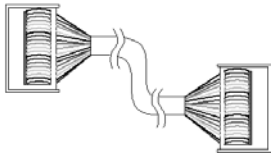
Signal Connections for DASP-52282

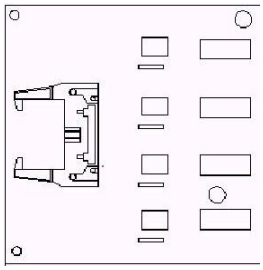
Referring to above figure, the accessories of the DASP-52282 are depicted and described as below.

- **CON1:**
  The I/O connector CON1 on the DASP-52282 is a 20-pin flat connector for digital input signals. CON1 enables you to connect to accessories, either the daughter board DB-87822 or the terminal block TB-88320, with the flat cable CB-89320-2 or CB-89320-5.
- **CON2:**
  The I/O connector CON2 on the DASP-52282 is a 20-pin flat connector for digital output signals. CON2 enables you to connect to accessories, either the daughter board DB-87825 or the terminal block TB-88320, with the flat cable CB-89320-2 or CB-89320-5.
- **CON3:**
  The I/O connector CON3 on the DASP-52282 is a JTAG test signal for internal usage only.
- **CON4:**
  The I/O connector CON4 on the DASP-52282 is a 37-pin D-sub connector for analog input and output signals. CON4 enables you to connect to accessory TB-88037 with the shielded cable CB-89037-2 or CB-89037-5.

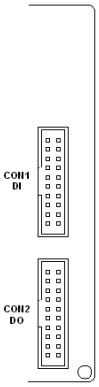
2.2.2 Digital Input Connector CON1

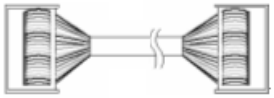


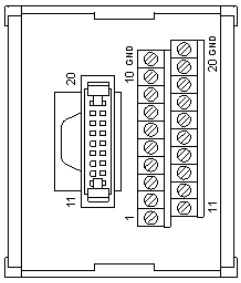




CON1 CB-89320 DB-87822







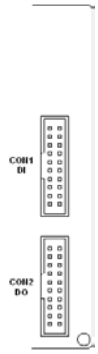
CON1 CB-89320 TB-88320

DI Signal Connections for DASP-52282

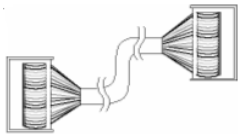
- **CON1: Digital Input Connector Pin Assignment (20-pin Flat Connector)**

Pin	Description	Pin	Description
1	Digital Input 0/TTL	2	Digital Input 1/TTL
3	Digital Input 2/TTL	4	Digital Input 3/TTL
5	Digital Input 4/TTL	6	Digital Input 5/TTL
7	Digital Input 6/TTL	8	Digital Input 7/TTL
9	Digital Input 8/TTL	10	Digital Input 9/TTL
11	Digital Input 10/TTL	12	Digital Input 11/TTL
13	Digital Input 12/TTL	14	Digital Input 13/TTL
15	Digital Input 14/TTL	16	Digital Input 15/TTL
17	PCB's GND	18	PCB's GND
19	PCB's +5V Output	20	PCB's +12V Output

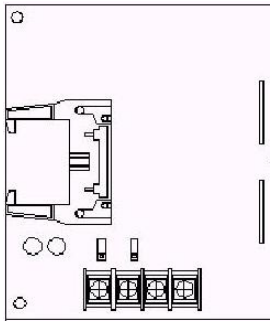
2.2.3 Digital Output Connector CON2



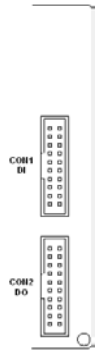
CON2



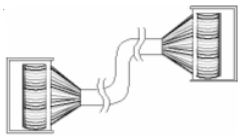
CB-89320



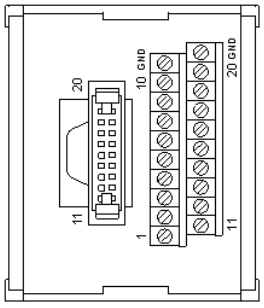
DB-87825



CON2



CB-89320



TB-88320

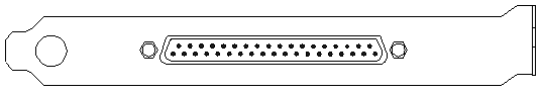
DO Signal Connections for DASP-52282

- **CON2: Digital Output Connector Pin Assignment (20-pin Flat Connector)**

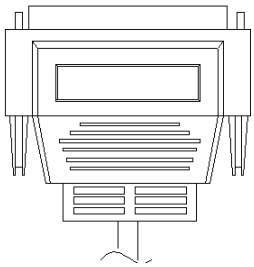
Pin	Description	Pin	Description
1	Digital Output 0/TTL	2	Digital Output 1/TTL
3	Digital Output 2/TTL	4	Digital Output 3/TTL
5	Digital Output 4/TTL	6	Digital Output 5/TTL
7	Digital Output 6/TTL	8	Digital Output 7/TTL
9	Digital Output 8/TTL	10	Digital Output 9/TTL
11	Digital Output 10/TTL	12	Digital Output 11/TTL
13	Digital Output 12/TTL	14	Digital Output 13/TTL
15	Digital Output 14/TTL	16	Digital Output 15/TTL
17	PCB's GND	18	PCB's GND
19	PCB's +5V Output	20	PCB's +12V Output

2.2.4 A/D, D/A and Timer/Counter Connector CON4

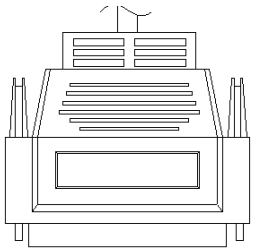
- **CON4: A/D, D/A and Timer/Counter Connector Pin Assignment**



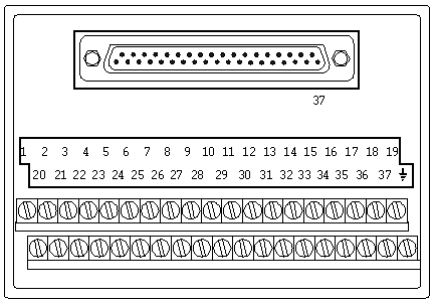
CON4



CB-89037



CB-89037



TB-88037

AIO Signal Connections for DASP-52282

D-Sub 37-pin Connector for Single-Ended Signal

Pin	Description	Pin	Description
1	Analog Input 0	20	Analog Input 8
2	Analog Input 1	21	Analog Input 9
3	Analog Input 2	22	Analog Input 10
4	Analog Input 3	23	Analog Input 11
5	Analog Input 4	24	Analog Input 12
6	Analog Input 5	25	Analog Input 13
7	Analog Input 6	26	Analog Input 14
8	Analog Input 7	27	Analog Input 15
9	Analog Ground	28	Analog Ground
10	Analog Ground	29	Analog Ground
11	No Connect	30	DAC 1 Output
12	No Connect	31	No Connect
13	+12V	32	DAC 2 Output
14	Analog Ground	33	No Connect
15	Digital Ground	34	No Connect
16	Timer/Counter 0 Output	35	No Connect
17	External Pulse Input	36	No Connect
18	OSC clock Out (8MHz)	37	External Clock Input
19	+5V		

- **CON4: A/D, D/A and Timer/Counter Connector Pin Assignment (D-Sub 37-pin Connector for Differential Signal)**

Pin	Description	Pin	Description
1	Analog Input 0/+	20	Analog Input 0/-
2	Analog Input 1/+	21	Analog Input 1/-
3	Analog Input 2/+	22	Analog Input 2/-
4	Analog Input 3/+	23	Analog Input 3/-
5	Analog Input 4/+	24	Analog Input 4/-
6	Analog Input 5/+	25	Analog Input 5/-
7	Analog Input 6/+	26	Analog Input 6/-
8	Analog Input 7/+	27	Analog Input 7/-
9	Analog Ground	28	Analog Ground
10	Analog Ground	29	Analog Ground
11	No Connect	30	DAC 1 Output
12	No Connect	31	No Connect
13	+12V	32	DAC 2 Output
14	Analog Ground	33	No Connect
15	Digital Ground	34	No Connect
16	Timer/Counter 0 Output	35	No Connect
17	External Pulse Input	36	No Connect
18	OSC clock Out (8MHz)	37	External Clock Input
19	+5V		

2.3 Jumper Setting

2.3.1 ADC Clock Source (JP4)

Pacer Tick Timer (8254 Counter1)

Jumper	External Clock	OSC Clock (8MHz) *	Cascade from 8254 COUT0
JP4	3-5	5-6	5-7

General Purpose Timer/Counter (8254 Counter0)

Jumper	External Clock	OSC clock (8MHz) *
JP4	1-2	2-4

2.3.2 DAC1, DAC2 Output Range Selection (JP8 and JP9)

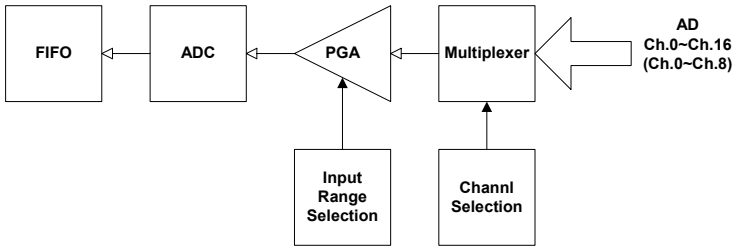
DAC Channel	Jumper	Output: 0V~+10V	Output: -10V~+10V *
Ch1	JP8	1-3 and 2-4	3-5 and 4-6
Ch2	JP9	1-3 and 2-4	3-5 and 4-6

2.3.3 A/D Single-Ended / Differential Selection (JP1)

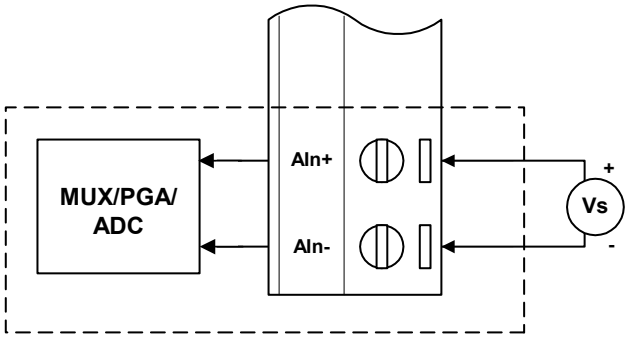
Jumper Name	Single-ended *	Differential
JP1	1-3 and 2-4	3-5 and 4-6

2.4 A/D, D/A and DI/DO Circuits and Wiring

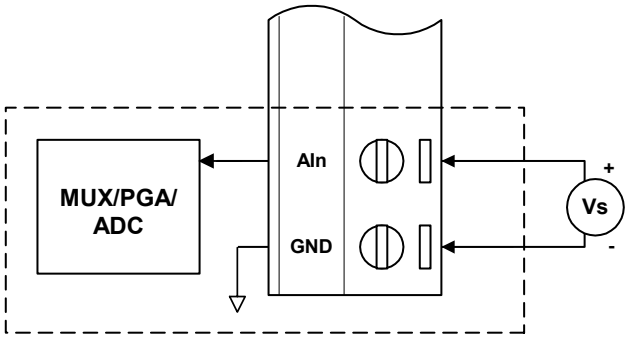
The analog input block diagram of DASP-52282 is depicted as in following figure. The analog input (differential and single-end input), digital input and digital output wirings are depicted as follows respectively.



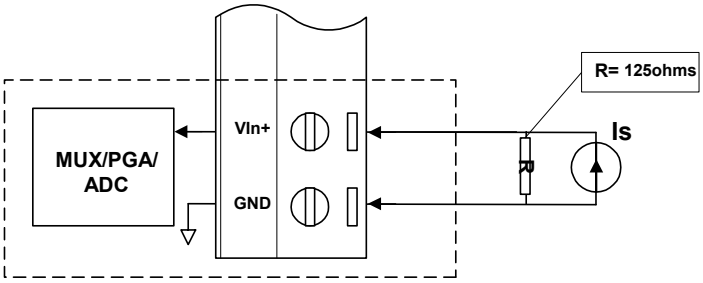
Analog Input Block Diagram for DASP-52282



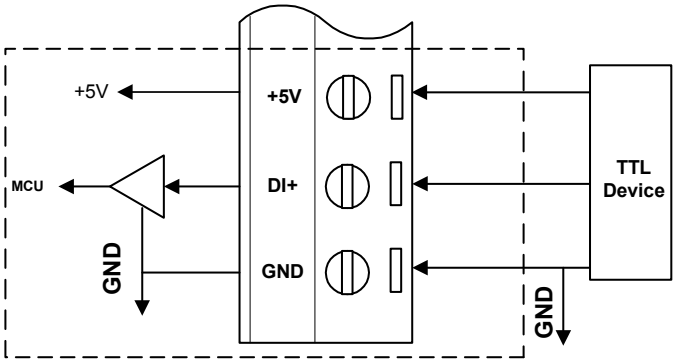
Analog Input Wiring Diagram for DASP-52282
(Differential Input)



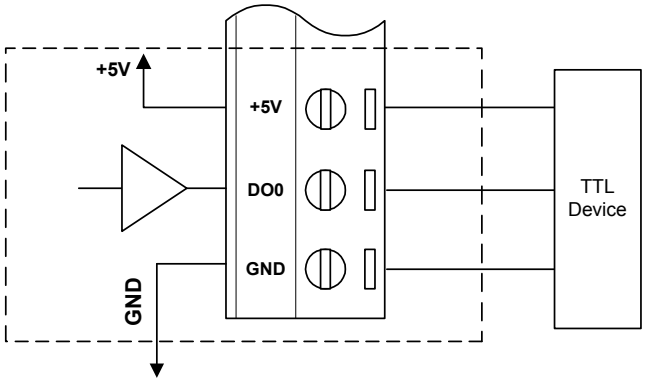
Analog Input Wiring Diagram for DASP-52282
(Single-End Input)



Analog Input Wiring Diagram for DASP-52282 (Current Input)



Digital Input Wiring Diagram for DASP-5228



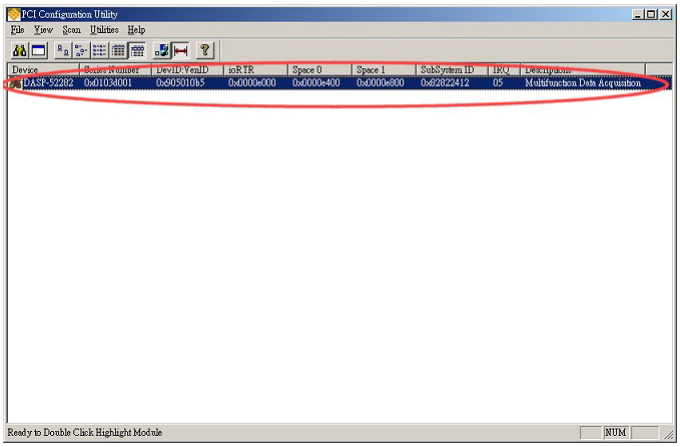
Digital Output Wiring Diagram for DASP-5228

2.5 Quick setup and test

To install a new DASP-52282 into an IBM PC compatible computer, at first, power-off the PC and open its chassis, then plug the DASP-52282 into a PCI slot. To fully benefit from the high data transfer efficiency of DASP-52282 during data acquisition, it is recommended not to install your DASP-52282 at the first PCI slot beside the AGP slot of the mainboard of PC. (The first PCI slot beside the AGP slot always shares the same IRQ with AGP device.) Based on the same consideration, please ensure that (the BIOS setting of) your PC has released enough IRQ resources for PCI devices. Do not share the same IRQ of DASP-52282 with other devices. The DASP-52282 is a plug and play device for MS Windows, and the OS will detect your DASP-52282 after you power on the PC. The detail of driver and software installation is described in software manual of DASP-52282.

After the hardware and software installation, user can emulate and test DASP-52282 step by step as follows.

- **Launch the 'PCI Configuration Utility' of DASP-52282 to ensure that the resource of DASP-52282 is properly dispatched by the OS. Press the scan button in the toolbar of 'PCI Configuration Utility' to find the installed DASP-52282, and then check the resource list as show in following figure.**

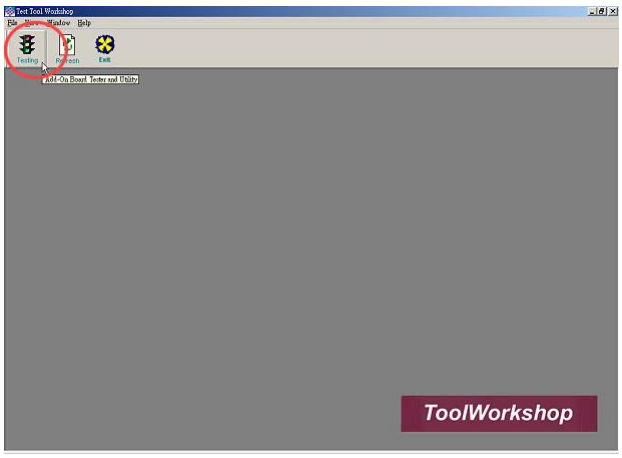


Scan DASP-52282 with PCI Configuration Utility and Check the Dispatched Resource

Check the dispatched resource of DASP-52282, take care the IRQ resource especially.

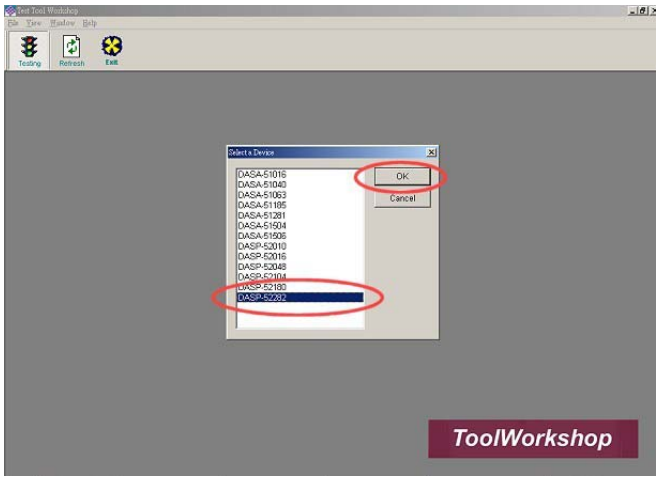
- **Exit the PCI Configuration Utility and launch the 'ToolWorkShop' for DASP-52282. As shown in following.**

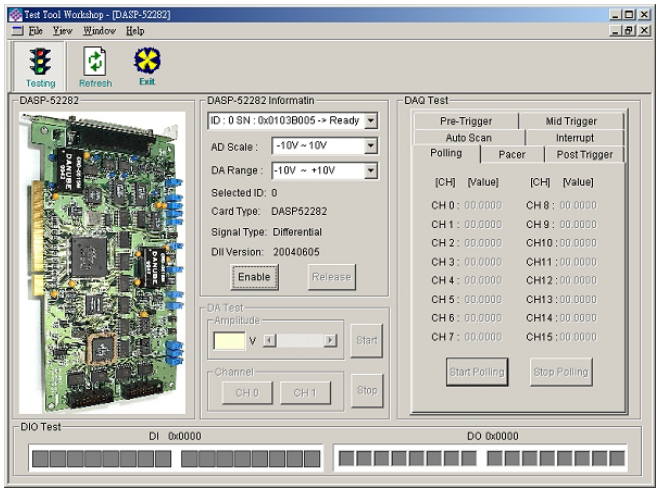
Launch ToolWorkShop



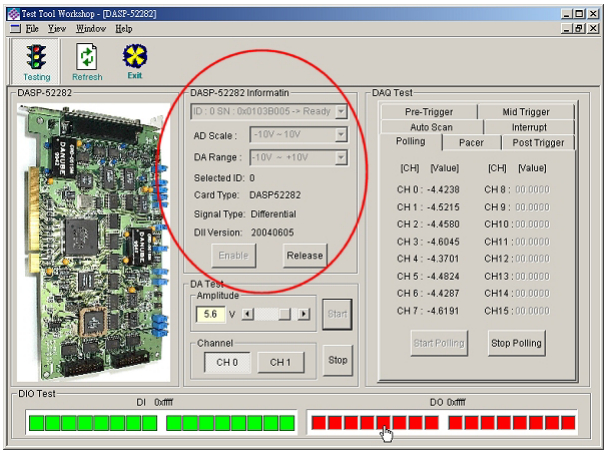
Select board test

- **Perform AD/DA and DIO test of DASP-52282 as shown in following.**

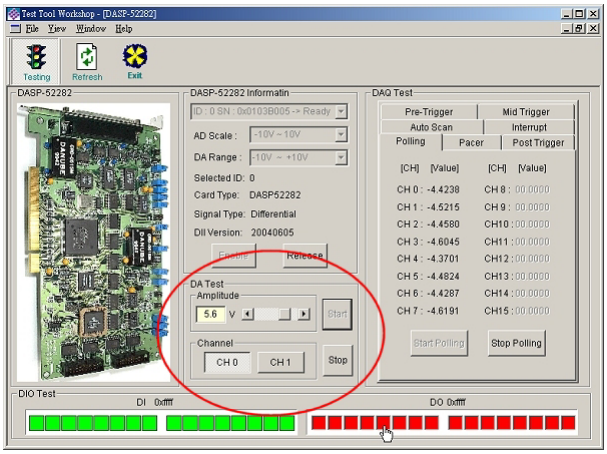




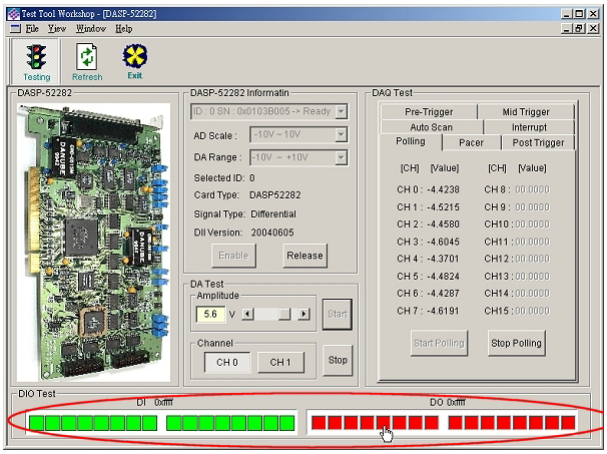
Select Test Target: DASP-52282



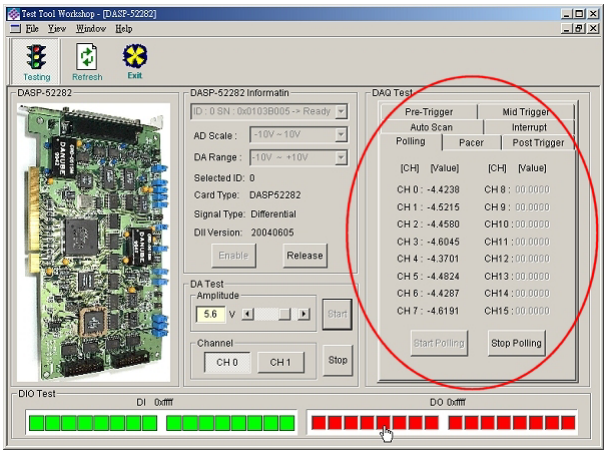
Check Device Information, Setup AO Range and Press 'Setup' Button to Load DASP-52282 Library



Perform Analog Output Test by Set the DA Value and Measure the Output Signal of DASP-52282 by Multi-meter



Perform DIO Test of DASP-52282, the DO of DASP-52282 Can be Routed to DI and Test Them by Commanded the DO Port Value and Read Back the DI Port Value. (DIO Wiring Refer to Section 2.4)



Perform the Analog Input Test of DASP-52282. A Reference Analog Input Signal can be Connected to AI Pins of Terminal Box of DASP-52282, Press ' Get' Button to Read Back AI Value.

- **Press 'Stop' button to stop AD converting. Before exiting ToolWorkShop, press 'Release' button to release DASP-52282 library.**

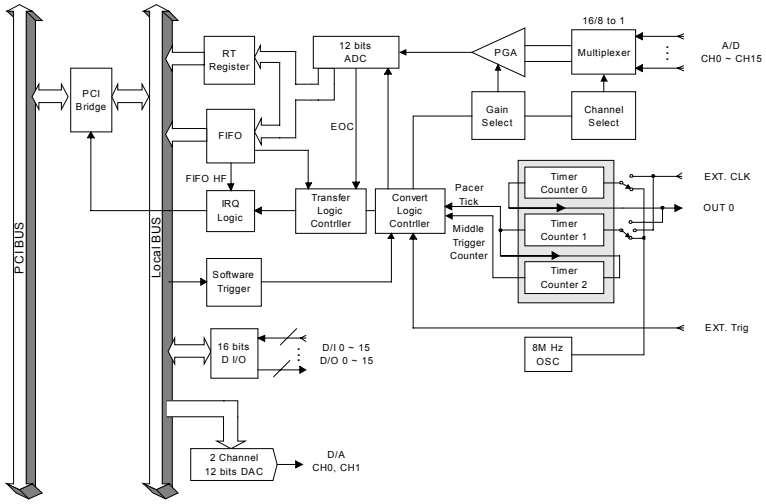
This page does not contain any information.

Chapter 3
Theorem of Operation

DASP-52282 is a high performance PCI interface multi-function data acquisition board. To facilitate high speed data acquisition and data transfer, a series of hardware and software mechanism has been designed and implemented for DASP-52282. To synchronize external event and data acquisition, a series of external trigger mechanism is provided. To guarantee the gapless data acquisition, a hardware/software level double buffering and a hardware level automatic channel scanning is supported. The theorem of these operations is described in the following sections. Please refer to the software manual of DASP-52282 for the details and practices of them.

3.1 Overview of DASP-52282 System Architecture and Operation

The system block diagram of DASP-52282 is depicted as in following figure. A PCI interface to host is constructed with a PCI bridge and a 33MHz bus clock is used to drive it. In the local bus site, 5 major functions of DASP-52282 have been implemented, include the AD circuits, the DA circuits, the DIO circuits, the internal control logical circuits and a FIFO buffer that provided the hardware level data buffering for double buffering mechanism of DASP-52282.



System Block Diagram of DASP-52282

3.2 Acquisition Modes of Analog Input

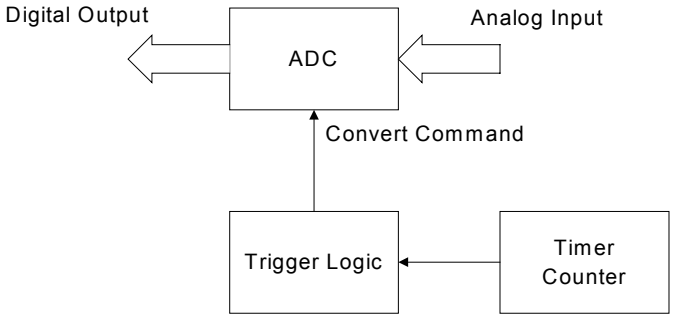
DASP-52282 provides internal (software/ hardware) trigger operation and external (hardware) trigger operation for data acquisition application. The supported internal trigger operations include a software polling mode and a hardware-clocked pacer mode. To synchronize external event and data acquisition of the DASP-52282, a series of external trigger mechanism, including pre-rigger, middle trigger and post trigger is provided. The operation mode of analog input of the DASP-52282 is described in the following subsections.

3.2.1 Polling Mode

With polling mode operation, according to the user's polling command, DASP-52282 performs an AD conversion of user specified analog input channel. To command DASP-52282 to perform a polling operation, write BASE+0x16 and ADC will convert one time. When AD conversion finish, **Pready** (BASE+0x02 Bit3) will be high.

3.2.2 Pacer Mode

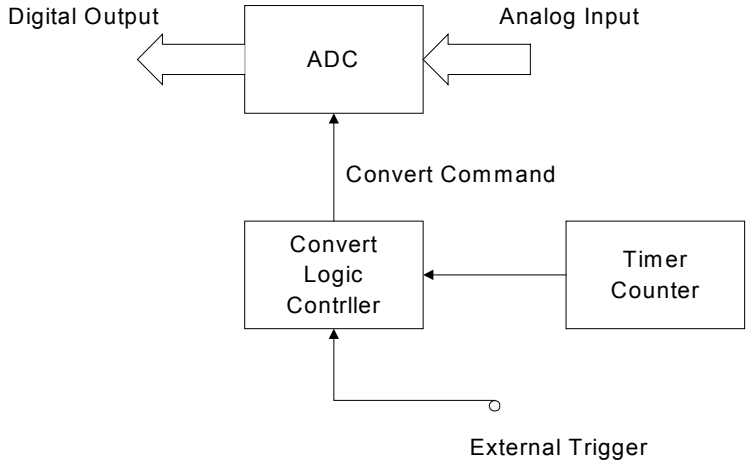
Benefited by the double buffering mechanism and the auto-scan mechanism, DASP-52282 can be operated at high sampling rate up to 330KHz. Instead of polling (software-commanded AD conversion), a series of hardware-clocked AD conversions can be performed to acquire data. The hardware pacer clock can be programmed from several Hz to 330KHz. With double buffering mechanism, the host program can retrieve batch data from the software buffer periodically. The only thing user need to consider is to retrieve buffered data frequently enough to prevent from the un-retrieved data in the buffer been overwritten. The functional block diagram of pacer mode operation of DASP-52282 is depicted as in following figure.



Functional Block Diagram of Pacer Mode Operation of DASP-52282

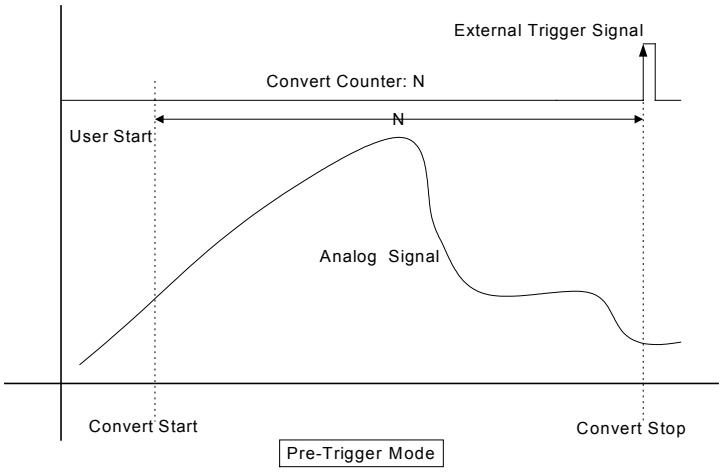
3.2.3 External Trigger Mode

To synchronize external event and data acquisition of the DASP-52282, a series of external trigger mechanism, including pre-trigger, middle trigger and post trigger, is provided. Based on the hardware pacer design described in 3.2.2 and the gate control logic for the hardware pacer clock, various external trigger mode operations of DASP-52282 are realized. According to the status of consumed external trigger signal and the amount of acquired data counted by hardware logic circuit, the gate control logic of AD conversion of DASP-52282 is emulates. With pre-trigger mode operation, DASP-52282 acquires and keeps the user specified amount of data before the external trigger signal fired. With the post trigger operation, DASP-52282 acquires and keeps the user specified amount of data after the external trigger signal fired. The functional block diagram of external trigger mode operation of DASP-52282 is depicted as below figure. Principles of pre-trigger and post-trigger are also shown in following.



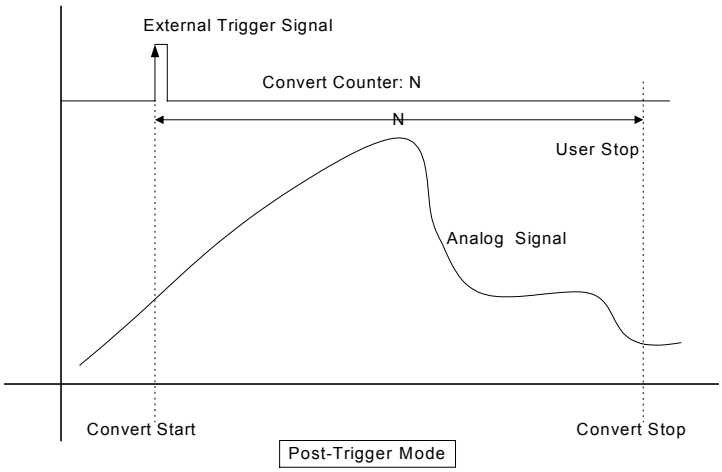
Functional Block Diagram of External Trigger of DASP-52282

Pre-Trigger Mode



Principle of External Pre-Trigger Operation of DASP-52282

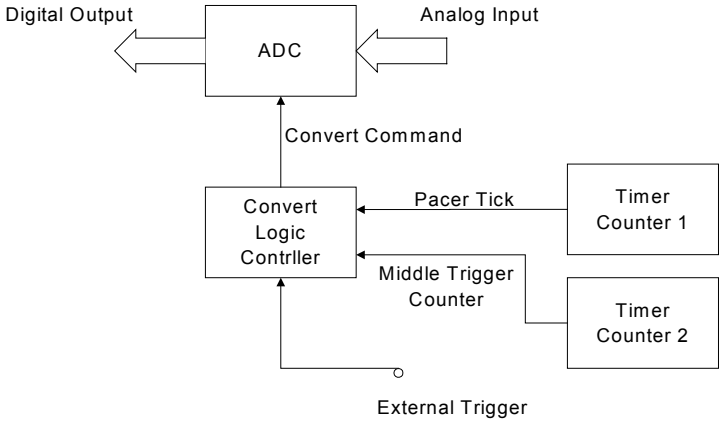
Post Trigger Mode



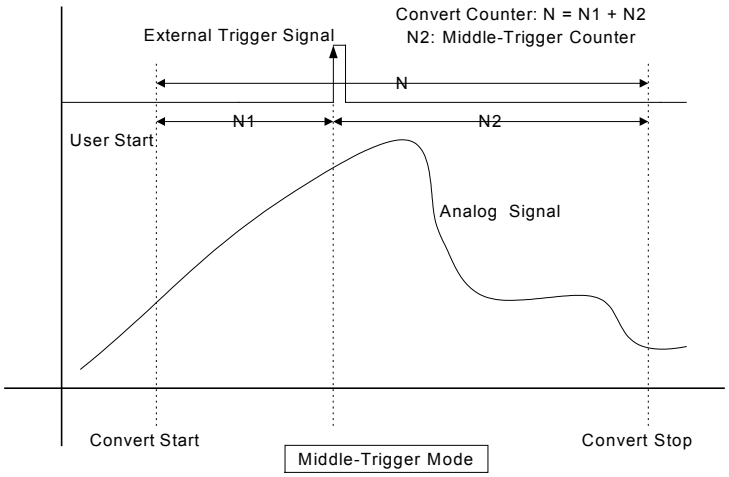
Principle of External Post-Trigger Operation of DASP-52282

Middle Trigger Mode

For middle trigger operation, DASP-52282 acquires and keeps user-specified amount of data before the external trigger signal fired, and continues to acquire and keep data after the external trigger signal fired till the user specified amount of data is acquired.



Functional Block Diagram of Middle-Trigger of DASP-52282



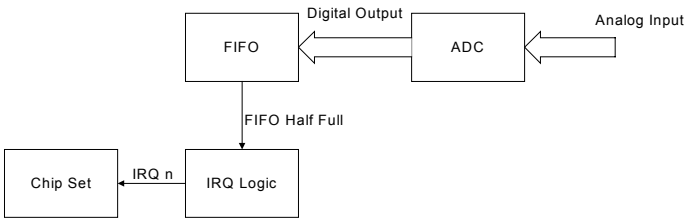
Principle of External Middle-Trigger Operation of DASP-52282

3.3 Double Buffering Mechanism For Fast Data Acquisition

To achieve gapless high speed data acquisition, a double buffering mechanism has been designed and realized for DASP-52282. The on board FIFO of DASP-52282 serves as the hardware level data buffers, and a 256K WORD software level data buffer is implemented by the ring 0 driver of DASP-52282.

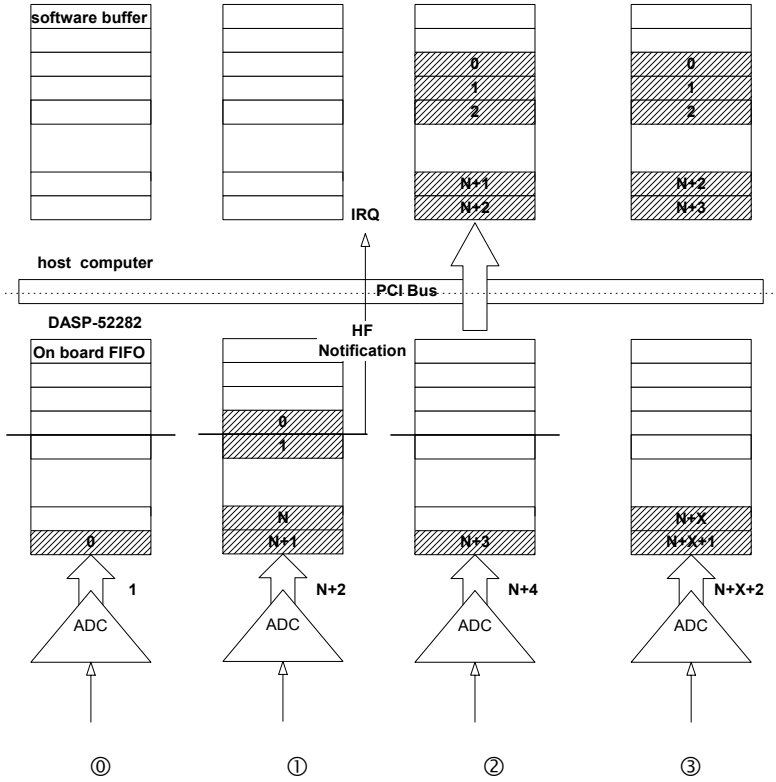
3.3.1 On Board FIFO and FIFO Half Full Interrupt

The DASP-52282 provides a 1K WORD on board FIFO (first in first out) buffer to support massive data transfer to its host. A FH (half-full) interrupt supported by the on board FIFO is used to launch batch data transfer mechanism of ring 0 driver of DASP-52282. The following shows the functional block diagram of massive data transfer of DASP-52282.



Functional Block Diagram of Massive Data Transfer of DASP-52282

When DASP-52282 is triggered to acquire data, the ADC samples the analog input signal and pushes the converted AD data to the on board FIFO. When free space of the on board FIFO is less than its half capacity, a HF signal is fired and the internal control logic of DASP-52282 produces an IRQ to the host. The FIFO HF IRQ in the host is dispatched to the ring 0 driver of DASP-52282, and a batch data transfer mechanism is launched to transfer the acquired data in on board FIFO of DASP-52282 to host, as show in following figure.



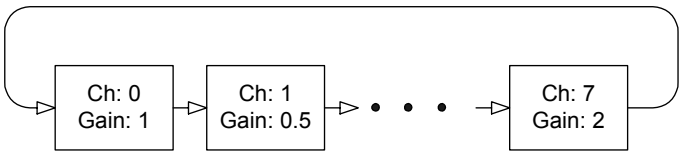
Principle of HF Interrupt Driven Massive Data Transfer of DASP-52282

3.3.2 Circular Buffer for Massive Data Buffering

To achieve the desired double buffering mechanism for DASP-52282, a 256K word ring 0 software buffer is constructed by the ring 0 driver of DASP-52282. The ring 0 software buffer serves as the second data buffer for massive data transfer between DASP-52282 and host computer. The ring 0 buffer operates as a circular buffer that will continuously update its contents and recursively overwrite the contents of the buffer when buffer is full. Incorporate with a header contains current status of the circular buffer, user can access the gapless acquired data through the provided ring 3 API.

3.4 Automatic Scan

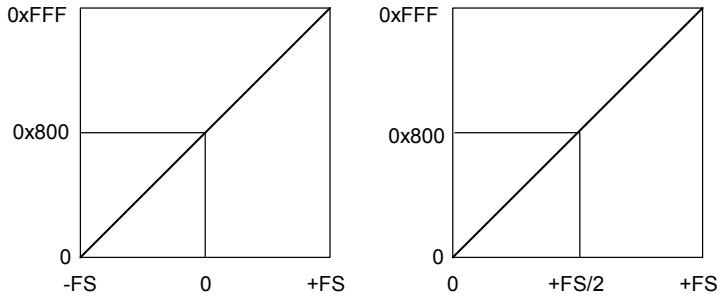
To perform high speed multi-channel data acquisition (or automatic scan), an on board micro controller is used to manipulate the input multiplexer and the PGA (programmable gain amplifier) of DASP-52282. Benefited by the capacity of embedded micro controller, DASP-52282 can perform high speed channel multiplexing and gain adjustment automatically. A sequence of instructions to perform automatic scan is stored in the on chip RAM of the micro controller, and can be software configured through a complete set of ring 3 API of DASP-52282. Figure 3-10 describes the principle of operation of auto scan schematically. The user configured auto scan instructions are stored into a queue structure, and the on board micro controller executes these instructions recursively when data acquisition is triggered.



Principle of Auto Scan.

3.5 Analog Input Range, ADC Code and AD Value

A almost linear mapping exist between the 12-bit ADC code and analog input for the DASP-52282, the nonlinearity of this linear mapping is described in section 1.2. Figure 4-6 depicts the linear mapping of AD code of DASP-52282 and the analog input signal. FS denotes the full span of analog input under the user configured analog input range. The mapping of analog input to ADC code of DASP-52282/ DASP-52282L/ DASP-52282H/ DASP-52282HL at ±FS and 0 input under different analog input ranges are listed in following respectively.



Mapping of 12-bit ADC Code and Analog Input for DASP-52282

Input range	+Full scale	Zero	-Full scale	Data resolution
±10V	+9.99512	±00.000	-10.000	0.00488V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±5V	+4.99756	±00.000	-5.000	0.00244V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±2.5V	+2.49878	±00.000	-2.5	0.00122V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±1.25V	+1.24939	±00.000	-1.25	0.00061V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±0.625V	+0.624695	±00.000	-0.625	0.000305
	0xFFF/4095	0x800/2048	0x0/0	1LSB

Input Range, Data/Code and Resolution of DASP 52282/ DASP 52282L – Bipolar Input

Input Range	+Full Scale	Zero	-Full Scale	Display Resolution
0~10V	+9.99756	±00.000	***	0.00244V
	0xFFF/4095	0x0/0	***	1LSB
0~5V	+4.99878	±00.000	***	0.00122V
	0xFFF/4095	0x0/0	***	1LSB
0~2.5V	+2.49939	±00.000	***	0.00061V
	0xFFF/4095	0x0/0	***	1LSB
0~1.25V	+1.249695	±00.000	***	0.000305
	0xFFF/4095	0x0/0	***	1LSB

Input Range, Data/Code and Resolution of DASP-52282 / DASP-52282L – Uni-Polar Input

Input Range	+Full Scale	Zero	-Full Scale	Data Resolution
±10V	+9.99512	±00.000	-10.000	0.00488V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±5V	+4.99756	±00.000	-5.000	0.00244V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±0.5V	+0.499756	±00.000	-0.5	0.000244V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±0.05V	+0.0499756	±00.000	-0.05	0.0000244V
	0xFFF/4095	0x800/2048	0x0/0	1LSB
±0.005 V	+0.00499756	±00.000	-0.005	0.00000244V
	0xFFF/4095	0x800/2048	0x0/0	1LSB

Input Range, Data/Code and Resolution of DASP-52282H / DASP-52282HL – Bipolar Input

Input Range	+Full Scale	Zero	-Full Scale	Display Resolution
0~10V	+9.99756	±00.000	***	0.00244V
	0xFFF/4095	0x0/0	***	1LSB
0~1V	+0.999756	±00.000	***	0.000244V
	0xFFF/4095	0x0/0	***	1LSB
0~0.1V	+0.0999756	±00.000	***	0.0000244V
	0xFFF/4095	0x0/0	***	1LSB
0~0.01V	+0.00999756	±00.000	***	0.0000244V
	0xFFF/4095	0x0/0	***	1LSB

Input Range, Data/Code and Resolution of DASP-52282H / DASP-52282HL – Uni-Polar Input

This page does not contain any information.

Chapter 4
Register Structure and Format

4.1 Overview

The DASP-52282 board occupies 16 consecutive I/O address. The address of each register is defined as the board's base address plus an offset. The I/O registers and their corresponding functions are listed in the followings.

Address	Read Function	Write Function
BASE+0x00	Digital Input (Low Byte)	Digital Output (Low Byte)
BASE+0x01	Digital Input (High Byte)	Digital Output (High Byte)
BASE+0x02	Status Register (Low Byte)	Command Register (Low Byte)
BASE+0x03	Status Register (High Byte)	Command Register (High Byte)
BASE+0x04	A/D Data Register (Low Byte)	D/A Channel 1 (Low Byte)
BASE+0x05	A/D Data Register (High Byte)	D/A Channel 1 (High Byte)
BASE+0x06	A/D FIFO Register (Low Byte)	D/A Channel 2 (Low Byte)
BASE+0x07	A/D FIFO Register (High Byte)	D/A Channel 2 (High Byte)
BASE+0x08	Read 8254 Counter 0	Load 8254 Counter 0
BASE+0x0A	Read 8254 Counter 1	Load 8254 Counter 1
BASE+0x0C	Read 8254 Counter 2	Load 8254 Counter 2
BASE+0x0E	Not Used	8254 Counter Control Words
BASE+0x10	Not Used	Clear FIFO Content
BASE+0x12	Not Used	Clear Flag
BASE+0x14	Not Used	Enable DAC1, DAC2 Output
BASE+0x16	Not Used	ADC Software Polling
BASE+0x18	Not Used	Enable ADC
BASE+0x1A	Not Used	Disable ADC

4.2 I/O Register Map

4.2.1 Digital Input Buffer Register

Read (Base Address + Offset 0x00-01)

D7	D6	D5	D4	D3	D2	D1	D0
Digital Input Low Byte (D0-D7)							

D15	D14	D13	D12	D11	D10	D9	D8
Digital Input High Byte (D8-D15)							

4.2.2 Digital Output Latch Register

Write (Base Address + Offset 0x00-01)

D7	D6	D5	D4	D3	D2	D1	D0
Digital Output Low Byte (D0-D7)							

D15	D14	D13	D12	D11	D10	D9	D8
Digital Output High Byte (D8-D15)							

4.2.3 General Status Buffer Register

Read (Base Address + Offset 0x02-03)

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{EnDAC}}$	Diff/SE	MidEnd	ExtPulse	PReady	$\overline{\text{FF}}$	$\overline{\text{HF}}$	$\overline{\text{EF}}$

D15	D14	D13	D12	D11	D10	D9	D8
CMDCRL	SetINT	OUT0	ModSel2	ModSel1	ModSel0	Handshak	CMDOK

General Status Buffer Register is used to check the A/D activity. The format is described as bellows.

- **EF:** (Bit 0 = 0) FIFO is Empty
- **HF:** (Bit 1 = 0) FIFO is Half-Full
- **FF:** (Bit 2 = 0) FIFO is Full
- **PReady:** (Bit 3 = 1) End of A/D Conversion
- **ExtPulse:** (Bit 4 = 1) External Trigger is active
- **MidEnd:** (Bit 5 = 1) End of External Middle Trigger
- **Diff/S.E.:**
  (Bit 6 = 1) Single-Ended; (Bit 6 = 0) Differential
- **EnDAC:**
  (Bit 7 = 0) Enable DAC1 and DAC2 output
- **CMDOK:**
  (Bit 8 = 1) PIC receive command and data are correct
- **Handshak:** (Bit 9 = 1) Setting Command to PIC
- **ModSel0,1,2:**
  (Bit 10,11,12) Selected ADC operation mode, refer to section 2.3.4 Mode0-2
- **OUT0:**
  (Bit 13 = 1) Status of 8254 Counter0 is high
- **SetINT:** (Bit 14 = 1) Interrupt event active
- **CMDCRL:**
  (Bit 15 = 1) Write command and data to PIC

4.2.4 Command Output Latch Register

Write (Base Address + Offset 0x02-03)

D7	D6	D5	D4	D3	D2	D1	D0
MUX3	MUX2	MUX1	MUX0	HDSK	Mode2	Mode1	Mode0

D15	D14	D13	D12	D11	D10	D9	D8
DevID	X	X	CMDOK	Ref1	Ref0	Gain1	Gain0

Command Output Latch Register is used to set the A/D operation. User must write high byte (bit8 - bit15) first. The format is described as bellows.

X: Don't care bits.

Mode0-2, HDSK: A/D Operation Mode Selection

Description	HDSK	Mode2	Mode1	Mode0
Polling Mode	0	0	0	0
Internal Pacer Mode	0	0	0	1
Interrupt Mode	0	0	1	0
External Pre-Trigger Mode	0	0	1	1
External Post Trigger Mode	0	1	0	1
External Middle Trigger Mode	0	1	1	1
Reversed	1	X	X	X

MUX0-3: A/D Multiplex Selection

- **A/D Input Channel Selection = MUX0~MUX3;**
- **MUX3 = MSB, MUX0 = LSB**
- **Single-Ended Mode = MUX0-MUX3 (Channel 0-15)**
- **Differential Mode = MUX0-MUX2 (Channel 0-7)**

- Single-Ended mode channel selection

Channel	MUX3	MUX2	MUX1	MUX0
Ch0	0	0	0	0
Ch1	0	0	0	1
Ch2	0	0	1	0
Ch3	0	0	1	1
Ch4	0	1	0	0
Ch5	0	1	0	1
Ch6	0	1	1	0
Ch7	0	1	1	1
Ch8	1	0	0	0
Ch9	1	0	0	1
Ch10	1	0	1	0
Ch11	1	0	1	1
Ch12	1	1	0	0
Ch13	1	1	0	1
Ch14	1	1	1	0
Ch15	1	1	1	1

- Differential mode channel selection

Channel	MUX2	MUX1	MUX0
Ch0	0	0	0
Ch1	0	0	1
Ch2	0	1	0
Ch3	0	1	1
Ch4	1	0	0
Ch5	1	0	1
Ch6	1	1	0
Ch7	1	1	1

- MUX3: Don't care bit in differential mode.

Gain0-1: A/D Gain Control (PGA205 or PGA206)

A/D GAIN	Gain0	Gain1
1x	0	0
2x	0	1
3x	1	0
4x	1	1

Ref0-1: A/D Reference Control

Instrumentation Gain	Ref0
1x	0
0.5x	1

Offset	Ref1
0V	0
5V	1

4.2.5 A/D Data Register

Read (Base Address + Offset 0x04-05)

D7	D6	D5	D4	D3	D2	D1	D0
AD Data (D0-D11)							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				AD Data (D0-D11)			

4.2.6 DAC Channel 1 Output Latch Register

Write (Base Address + Offset 0x04-05)

D7	D6	D5	D4	D3	D2	D1	D0
DA Data to Channel 1 (D0-D11)							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				DA Data to Channel 1 (D0-D11)			

4.2.7 A/D FIFO Data Register

Read (Base Address + Offset 0x06-07)

D7	D6	D5	D4	D3	D2	D1	D0
AD FIFO Data (D0-D11)							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				AD FIFO Data (D0-D11)			

4.2.8 DAC Channel 2 Output Latch Register

Write (Base Address + Offset 0x06-07)

D7	D6	D5	D4	D3	D2	D1	D0
DA Data to Channel 2 (D0-D11)							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved				DA Data to Channel 2 (D0-D11)			

4.2.9 8254 Timer/Counter Register

Read/ Write (Base Address + Offset 0x08-0C)

D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8
8254 Counter 0, 1, and 2							

Please refer to Intel's "Micro-system Components Handbook" for detailed.

4.2.10 8254 Timer/Counter Control Words Register

Write (Base Address + Offset 0x0E)

D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8
8254 Control Words							

Please refer to Intel's "Micro-system Components Handbook" for detailed.

4.2.11 Clear FIFO Content Register

Write (Base Address + Offset 0x10)

D7	D6	D5	D4	D3	D2	D1	D0
Write Any Value to Clear FIFO Content							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

4.2.12 Clear Flag Register

Write (Base Address + Offset 0x12)

D7	D6	D5	D4	D3	D2	D1	D0
Write Any Value to Reset the System Status to Initial State							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

4.2.13 Enable DAC1 and DAC2 Output Register

Write (Base Address + Offset 0x14)

D7	D6	D5	D4	D3	D2	D1	D0
Write Any Value to Enable DAC1 and DAC2							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

4.2.14 A/D ADC Software Polling Control Register

Write (Base Address + Offset 0x16)

D7	D6	D5	D4	D3	D2	D1	D0
Write Any Value to Generate an AD Conversion Signal							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

Write this register to any value to generate a Conversion Signal and the **PReady** Bit (Status Register Bit 3) will be set to TRUE.

4.2.15 Enable ADC Register

Write (Base Address + Offset 0x18)

D7	D6	D5	D4	D3	D2	D1	D0
Write Any Value to Enable AD Conversion							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

4.2.16 Disable ADC Register

Write (Base Address + Offset 0x1A)

D7	D6	D5	D4	D3	D2	D1	D0
Write Any Value to Disable AD Conversion							

D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

Chapter 5
Calibration

5.1 Calibration VR Description

There are ten variable resistors (VR) on the DASP-52282 to adjust the A/D and D/A channels. A precision voltmeter with 4 1/2 digits should be used to take an accurate voltage reference. A calibration program can be found on the DASP-52282 software disk to perform the calibration steps. It is strongly recommended to warm up the computer 30 minute before performing calibration. Locations of individual VR are shown in Chapter 2. The corresponding VR's function is depicted as below.

VR Number	Description
VR1	Reserved
VR2	ADC Analog Input Span Adjustment
VR3	ADC Bipolar Analog Input Offset Adjustment
VR4	ADC Unipolar Analog Input Offset Adjustment
VR5	DAC Channel 1 Bipolar Offset Adjustment
VR6	DAC Channel 1 Unipolar Offset Adjustment
VR7	DAC Channel 2 Unipolar Offset Adjustment
VR8	DAC Channel 2 Bipolar Offset Adjustment
VR9	DAC Channel 1 Span Adjustment
VR10	DAC Channel 2 Span Adjustment

5.2 D/A Calibration

Calibration procedure is easily performed by using the calibration program. Step-by-step walkthrough of D/A calibration is listed as follows:

- **Select DAC1 (JP8) and DAC2 (JP9) to ±10V output range**
- **Set DAC1 and DAC2 output data to -10V and adjust VR5, VR8 until DAC1 and DAC2 output voltage to -10V with 1 LSB tolerance (±2.44mV)**
- **Set DAC1 and DAC2 output voltage to +10V and adjust VR9, VR10 until DAC1, DAC2 output voltage to +10V with 1 LSB tolerance**
- **Select DAC1 (JP8) and DAC2 (JP9) to 0~10V output range**
- **Set DAC1 and DAC2 output voltage to 0V, adjust VR6 and VR7 until DAC1 and DAC2 output voltage to 0V with 1 LSB tolerance, respectively**
- **Set DAC1 and DAC2 output voltage to 10V, adjust VR9 and VR10 until DAC1 and DAC2 output voltage to 10V with 1 LSB tolerance, respectively**

5.3 A/D Calibration Steps

Calibration procedure is easily performed by using the calibration program. Step-by-step walkthrough of A/D calibration is listed as follows:

- **Connect A/D input channel 0 to ground (0V)**
- **Select bipolar input configuration, adjust VR3 until ADC reading value to zero with 0.5 LSB tolerances (±1.22mV)**
- **Select unipolar input configuration, adjust VR4 until ADC reading value to zero with 0.5 LSB tolerances (±1.22mV)**
- **Connect A/D input channel 0 to a DC voltage source +5V (or directly connect to D/A output +5V)**
- **Adjust VR2 until ADC reading data to +5V with 1 LSB tolerance (±2.44mV)**

Appendix A
Analog Input Gain Mode Configuration

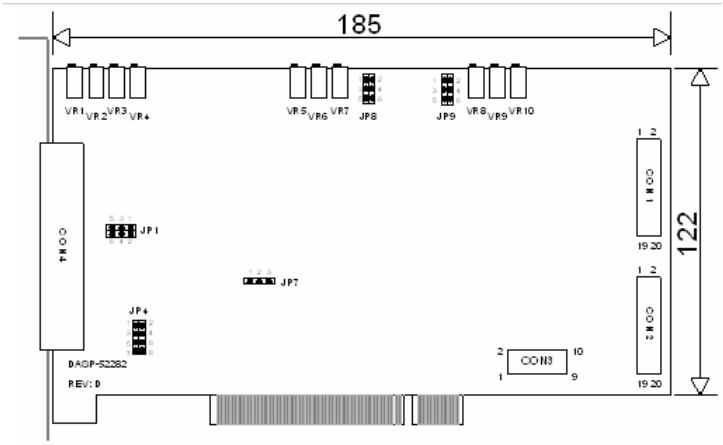
Command Register High Byte bit11~ bit8				Gain Mode	Gain	Type	Input Range	Full Range
Ref1	Ref0	Gain1	Gain0					
0	0	0	0	0	1 x	Bipolar	±5V	10V
0	0	0	1	1	2 x	Bipolar	±2.5V	5V
0	0	1	0	2	4 x	Bipolar	±1.25V	2.5V
0	0	1	1	3	8 x	Bipolar	±0.625V	1.25V
0	1	0	0	4	0.5 x	Bipolar	±10V	20V
1	0	0	0	8	1 x	Unipolar	0 ~ 10V	10V
1	0	0	1	9	2 x	Unipolar	0 ~ 5V	5V
1	0	1	0	10	4 x	Unipolar	0 ~ 2.5V	2.5V
1	0	1	1	11	8 x	Unipolar	0 ~ 1.25V	1.25V

User could fill the **Gain Mode** in this table into PCI828x_SetADConfig() function in the driver DLL to set the analog input range configuration.

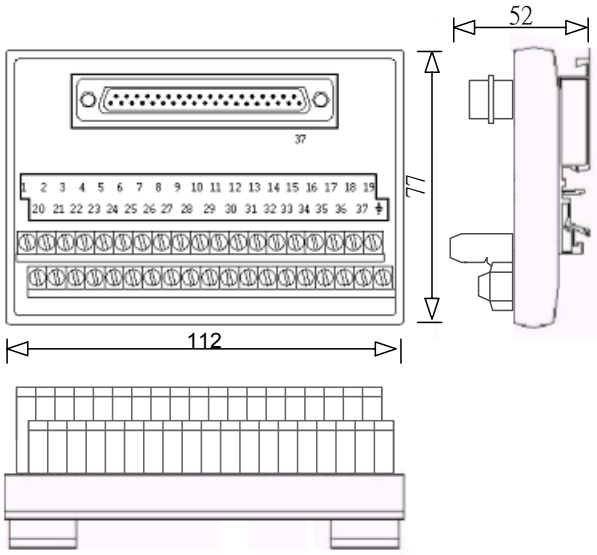
This page does not contain any information.

Appendix B
Dimension of DASP-52282 and Accessories

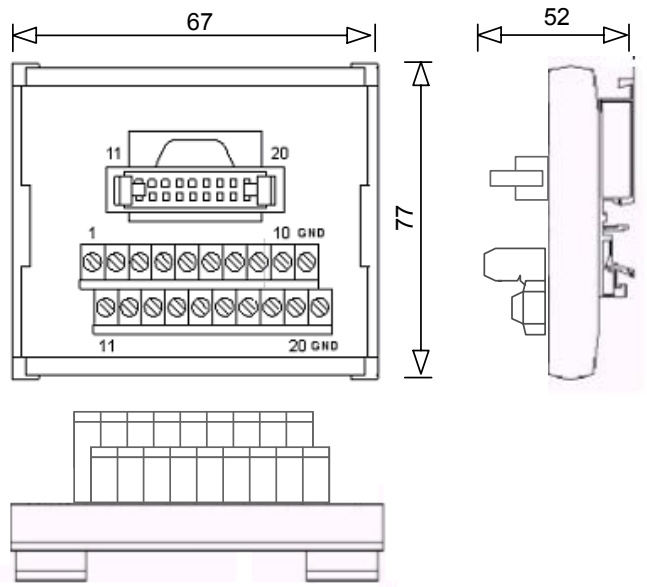
- **DASP-52282**



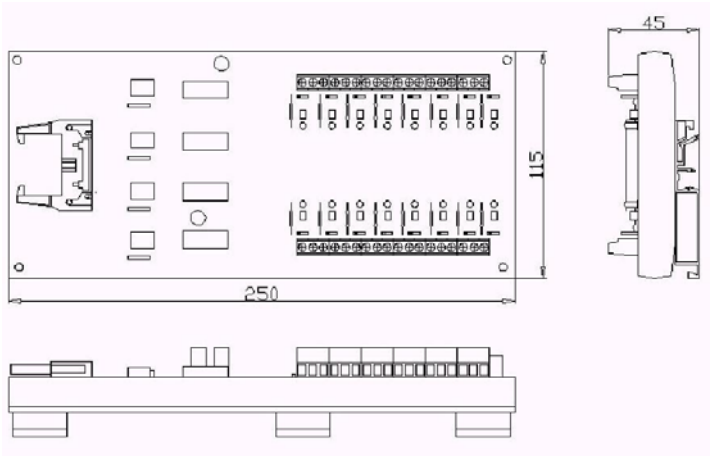
- **TB-88037**



- **TB-88320**



- **DB-87822**



- **DB-87825**